Remarks

Claims 1-15 are pending in this action. Claims 1-15 stand rejected. By this amendment claims 1-2, 7, and 11 have been amended and claim 6 has been canceled. Applicants respectfully request reconsideration of all pending claims herein.

Claim Objections

The Office Action stated that Claims 1 – 15 are objected to because "a memory block located at each of the cross points" is unclear because memory location seems to be irrelevant in the claim, contrary to the memory connection/association to the ports as claimed. Applicants have amended Claim 1 to clarify that a memory block is associated with an input port and an output port and is not dependent on physical location. Claim 1 now reads, "...wherein the packet switch comprises a memory block *for* each of the cross points".

Claim Rejections - 35 U.S.C. § 112 Second Paragraph

The Office Action stated that claims 1-15 are rejected under U.S.C. 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Specifically, for Claim 1, the Office Action stated that it was unclear as to what output and input ports are considered a pair and what is the definition of a cross point. Applicants submit that the definition of "cross point" is defined in paragraph 10 of the specification as "each couple of an input port and an output port defining a cross point within the switch module" and also shown in Figures 1, 3, 5, and 8. In Figure 1, the input and output ports are shown as the input buses 13_1 – 13_4 and corresponding output busses 15_1 – 15_4 coupled to the packet switch module 14. A pair is therefore any one of the input ports (i.e. input bus 13) coupled to any one of the output ports (i.e. output bus 15). For example, one cross point is input bus 13_1 coupled to output bus 15_4, or input bus 13_2 coupled to output bus 15_3, etc. Thus, for 4 input ports and 4 output ports there is a total of 16 cross points. In Figure 3 the cross point is shown as the intersection of elements 50 and 60, which are coupled to data bus in 13 and data bus out 15

respectively (see paragraph 27). Memory Block 200 is associated with the cross point shown in Figure 3. Figure 5 shows a block diagram of Memory Block 200 with the intersection of elements 50 and 60 showing the cross point. Figure 8 shows multiple cross points for input ports 13_1 – 13_m and output ports 15_1 – 15_m and represents an mxm number of cross points with associated memory blocks 200 for each cross point.

Claims 1 and 2 were objected to because the meaning of "forwarding... at each clock time" is unclear with respect to when the forwarding should occur because there are no time units associated with "each clock time". Applicants have amended "each clock time" to "each clock cycle", which is a well-known term in the networking and computer industries.

The Office Action stated that the limitation of Claim 1, "a data controller which forwards to the output port a data packet stored in a data memory unit of a memory block corresponding to the output port" is unclear because it is not understood whether the data packet or the memory block corresponds to the output port. Applicant's have amended Claim 1 to read, "a data controller which forwards the data packet to an output port which corresponds to the memory block" to clarify that the memory block corresponds to the output port.

The Office Action stated that Claim 11 is rejected because there is a lack of antecedent basis for the limitation "the fourth memory controller". Applicants have amended Claim 11 to provide the proper antecedent basis.

Based on the foregoing arguments and amendments, Applicants submit that the rejection to Claims 1 – 15 under 35 U.S.C. §112 second paragraph, has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that claims 1, 2, 4 and 11 are rejected under 35 U.S.C. § 103(a),

as being unpatentable over U.S. Patent No. 6,205,145 issued to Yamazaki because Yamazaki teaches a data transmission system having a plurality of networks interconnected by a hub, including a plurality of adapters respectively connected to the plurality of networks, comprising a packet switch and a data packet containing an adapter address. The packet switch further comprises a memory block corresponding to a cross point.

The Office Action stated that Yamazaki does not teach networks such as LANs and locating memory blocks at each cross point; but that it would have been obvious to one of ordinary skill in the art at the time the invention was made to add LANs and locating memory blocks at each cross point to the system of Yamazaki to incorporate well known and popular type of networks into the system.

Applicants respectfully submit that the present invention is patentable over U.S. Patent No. 6,205,145 issued to Yamazaki because Yamazaki does not teach "a cross point within the packet switch module, wherein the packet switch comprises a memory block for each of the cross points" as described in Applicants' claim 1 (See Benayoun Figures 5, and 8, paragraphs 0027 and 0033, and claim 1). The combination of input and output buffer means shown as 20-23 and 30-33 respectively on Fig. 5 of the Yamazaki reference are not cross points because there is no provision for each input/output buffer combinations to coordinate one-to-one with every termination node input/output node combination. Yamazaki does not teach a memory block for each of the cross points because cell producing means 40-43 does not include a first memory controller which determines from the packet header whether the packet is to be forwarded to the output port associated with the cross point. Rather, the frame division control section 143 of Figure 8 (referred to in the Office Action) serves to divide an incoming packet into fixed length cells, interchange the cells and, reconstruct the original frame from the interchanged cells (See Yamazaki Abstract, Summary, Claims 1, 6, 10, 16, 26, and 29, Figure 8, and 10:57-11:4). The output buffer requirement control section 144 of Figure 8 sends command signals the frame division control 143 according to inputs from the congestion control bus 180 (See Yamazaki 10:14-26, and Figures 6 and 8). Neither the output buffer requirement control section 144 nor the frame division control section 143 determine from the packet header whether the packet is to be forwarded to the output

port associated with the cross point as taught by the Applicants' instant invention. Therefore, Applicants' respectfully submit that the rejection of independent Claim 1 under 35 U.S.C. §103(a) has been overcome, thereby also removing rejections to dependent Claims 2, 4, and 11.

The Office Action also stated that Claims 6 and 7 are rejected under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,205,145 issued to Yamazaki in view of U.S. Patent No. 5,233,603 issued to Takeuchi. The Office Action submitted that Yamazaki does not teach an input control block comprising an input memory unit connected to each input port for buffering a data packet before transmitting the data packet over a distribution bus connected to all memory blocks corresponding to the input port and a third memory controller storing the packets into the input memory unit and reading them out over the bus.

The Office Action stated that Takeuchi teaches an input control block comprising an input memory unit connected to each input port for buffering a data packet before transmitting the data packet over a distribution bus connected to all memory blocks corresponding to the input port and a third memory controller storing the packets into the input memory unit and reading them out over the bus; and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to add an input control block to improve system reliability and speed using multiple memory blocks.

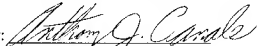
Applicants have canceled Claim 6 and amended Claim 7 to further include the limitation set forth in Claim 6. Applicants respectfully submit that the invention described in Yamazaki in view of Takeuchi does not read on Applicant's Claim 7 as amended because Applicants recite a third controller which controls the data memory unit and the buffer using read, write, validation, and fill-level signals (see, for example: Benayoun Figure 4, paragraph 29, Claim 7). A controller that performs such functions is not present in Yamazaki nor Takeuchi, nor do the references provide motivation to add a such a controller. Therefore, Applicants respectfully submit that the rejection of Claims 6 and 7 under 35 U.S.C. § 103(a) has been overcome by the foregoing amendments and that Claim 7 is in condition for allowance.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Alain Benayoun, et al.

By: 

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